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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/471,877	SFARTI ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-14,16,17 and 20-33* is/are pending in the application.

4a) Of the above claim(s) *1-6,15,18,19 and 28-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,10,11,14 and 17* is/are rejected.

7)☒ Claim(s) *8,9,12,13 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/14/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claims 7-14,16,17,20-27 are presented for examination. Claim 1-6,15,18,19,28-33 have been canceled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7,10,11,14,17 are rejected under 35 U.S.C. 103(a) as being unpatentable over So (5,909,559) in view of Watts (6,023,587).

So taught a system including at least :
a central processing unit (CPU106 Fig.1) operable to execute operational instructions, wherein the central processing unit includes an arithmetic logic unit (CPU MMX) interoperably coupled with a data module, an instruction module, wherein the central processing unit issues a memory access request when information relating to executing one of the operational instructions is not stored within the data module or the instruction module (see the IO request and data buffer in col.39, lines 13-60, see also DRAM controller and the arbiter in col.3, lines 11-30, see PCI request from CPU in col.19, lines 9-30) , and wherein the central processing unit is contained on a substrate; north bridge [North bridge 108] operably coupled to interface with memory (cache or Main memory) at a memory rate, wherein the north bridge includes a memory access request buffer interoperably coupled with a memory controller (see the RAM and the PCI bus master in col.37, lines 39-67, col.38, lines 1-50), wherein the memory access request buffer receives the memory access request from the central processing unit at the operating rate of the central processing unit, wherein the memory controller retrieves the memory access request from the memory access request buffer (see the

IO request and data buffer in col.39, lines 13-60, see also DRAM controller and the arbiter in col.3, lines 11-30, see PCI request from CPU in col.19, lines 9-30) at the memory rate (memory rate not explicitly shown, but must be memory rate otherwise would not be operative), wherein the memory controller processes the memory access request to produce a memory response that includes information stored in memory (see request queue and PCI transactions in col.37, lines 39-67, col.38, lines 1-8), and wherein the north bridge is contained on the substrate (see integrated circuits in col.2, lines 4-8 for background, see also ASIC in col.16, lines 29-35, see also all processors and bus suitably fabbed on single chip in col.15, line 32); and,
a bus operably coupled to the central processing unit [CPU 106] and the north bridge (see connection between CPU 106 and north bridge 108 in fig.1), wherein the bus provides a transport medium for memory access requests and corresponding memory responses between the central processing unit and the north bridge at the operating rate of the central processing unit (not explicitly shown, but see CPU MMX operating rate as known in the art) , and wherein the bus is contained on the substrate.

So did not specifically show the programmable phase locked loop that provides an operating rate for the central processing unit. However, Watts Jr (6,023,587) taught programmable phase locked loop that provides an operating rate for the central processing unit [CPU] (see the clock rate pf phase locked loop to CPU in col.14, lines 43-47). It would have been obvious to one of ordinary skill in the art to use Watts in So for including the programmable phase locked loop that provides an operating rate for the central processing unit as claimed because the use of Watts could provide So the ability to control the clock intervals at a predefined set of system requirement, and one of ordinary skill in the art should be able to recognize the advantage of using the programmable phase locked loop as adjustable CPU internal cock.
As to claims 10,17, So did not specifically show the physical address as claimed. However, since no specific format of physical address has been reflected in the claim, examiner holds that generation of physical address in general had been known in the art.

As to claim 11, So also included a memory bus coupled to north bridge (see bus connected to the north bridge and the memory in fig.1).

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the data module comprises operable coupling to a data portion of the bus, wherein the data module provides data memory access requests via the data portion of the bus to the north bridge and wherein the memory access request buffer further comprises a data portion operable coupled to receive the data memory access requests from the data portion of the bus.

Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the instruction module comprises operable coupling to an instruction portion of the bus, wherein the instruction module provides instruction memory access requests via the instruction portion of the bus to the north bridge and wherein the memory access request buffer further comprises an instruction portion operably coupled to receive the instruction memory access requests from the instruction portion of the bus.

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the device bus that is contained on the substrate, wherein the device bus couples the north bridge to south bridge that is contained on the substrate.

Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the graphics controller that is contained on the substrate, wherein the graphics controller includes a frame buffer controller for processing data transferences between

the graphics controller and a frame buffer and wherein the graphics controller issues a graphics memory access request to the north bridge.

Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the central processing unit further comprises an address generation unit that generates the memory access request to include an address in virtual memory address space, and wherein the north bridge further comprises an address translation module operably coupled to translate the address from the virtual memory space to an address in physical memory space.

As to claims 20-27, none of the prior art of record teaches the combined features of the integrated personal computing system comprising the central processing unit operable to execute operational instructions, the central processing unit includes an arithmetic logic unit interoperably coupled with a data module, an instruction module, the programmable phase locked loop provides an operating rate for the central processing unit, and issues a memory access request when information relating to executing one of the operational instructions is not stored within the data module or the instruction module, the central processing unit is contained on a substrate, the north bridge operably coupled to interface with memory at a memory rate and includes a memory access request buffer interoperably coupled with a memory controller, the memory access request buffer receives the memory access request from the central processing unit at the operating rate of the central processing unit, the memory controller retrieves the memory access request from the request buffer at the memory rate, the memory controller processes the memory access request to produce a memory response that includes information stored in memory, the north bridge contained on the substrate; the bus operably coupled to the central processing unit and the north bridge, and provides a transport medium for memory access requests and corresponding memory responses between the central processing unit and the north bridge at the operating rate of the central processing unit, the bus contained on the

substrate, the south bridge contained on the substrate, and provides an interface between the external device and the north bridge, the device bus contained on the substrate, and coupled the north bridge to the south bridge.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wandler et al. (5,991,833) is cited for the teaching of north bridge and the buffer request at CPU rate (see col.6, lines 17-22, col.11, lines 55-67, col.12, lines 1-25, see fig.2 CPU BUS)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

/Daniel Pan/
Primary Examiner, Art Unit 2183